MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

Document order number: MC33887/D
Rev 6.0, 03/2003

Advance Information

33887

5.2 A H-Bridge with Load Current Feedback

5.2 A H-BRIDGE WITH LOAD CURRENT FEEDBACK

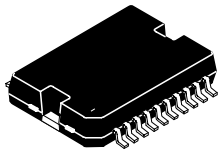
The 33887 is a monolithic H-Bridge Power IC with a load current feedback feature making it ideal for closed-loop DC motor control. The IC incorporates internal control logic, charge pump, gate drive, and low $R_{DS(ON)}$ MOSFET output circuitry. The 33887 is able to control inductive loads with continuous DC load currents up to 5.2 A, and with peak-current active-limiting between 5.2 A and 7.8 A. Output loads can be pulse width modulated (PWM-ed) at frequencies up to 10 kHz. The load current feedback feature provides a proportional (1/375th of the load current) constant-current output suitable for monitoring by a microcontroller's A/D input. This feature facilitates the design of closed-loop torque control.

A Fault Status output reports undervoltage, overcurrent, and overtemperature conditions. Two independent inputs provide polarity control of two half-bridge totem-pole outputs. Two disable inputs force the H-Bridge outputs to tristate (exhibiting high impedance).

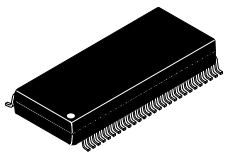
The 33887 is parametrically specified over a temperature range of -40°C ≤ T_A ≤ 125°C and a voltage range of 5.0 V ≤ V_{PWR} ≤ 28 V. The IC can also be operated for short periods of time at 150°C and up to 36 V with derating of the specifications.

Features

- 5.0 V to 28 V Continuous Operation
- 120 mΩ $R_{DS(ON)}$ H-Bridge MOSFETs
- TTL/CMOS Compatible Inputs
- PWM Frequencies up to 10 kHz
- Automatic Overcurrent Limiting via Internal Constant-Off-Time PWM
- Output Short Circuit Protection with Shutdown
- Temperature-Dependant Current-Limit-Threshold Reduction
- Undervoltage Shutdown
- Fault Status Reporting
- Sleep Mode with Current Draw ≤50 µA



DH SUFFIX
PLASTIC PACKAGE
20-LEAD HSOP
CASE 979C

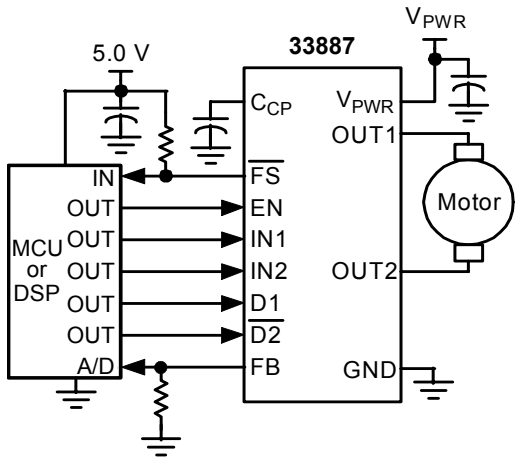


DWB SUFFIX
PLASTIC PACKAGE
54-LEAD SOICW-EP
CASE 1390

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MC33887DH/R2	-40 to 125°C	20 HSOP
MC33887DWB/R2	-40 to 125°C	54 SOICW-EP

33887 Simplified Application Diagram



This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

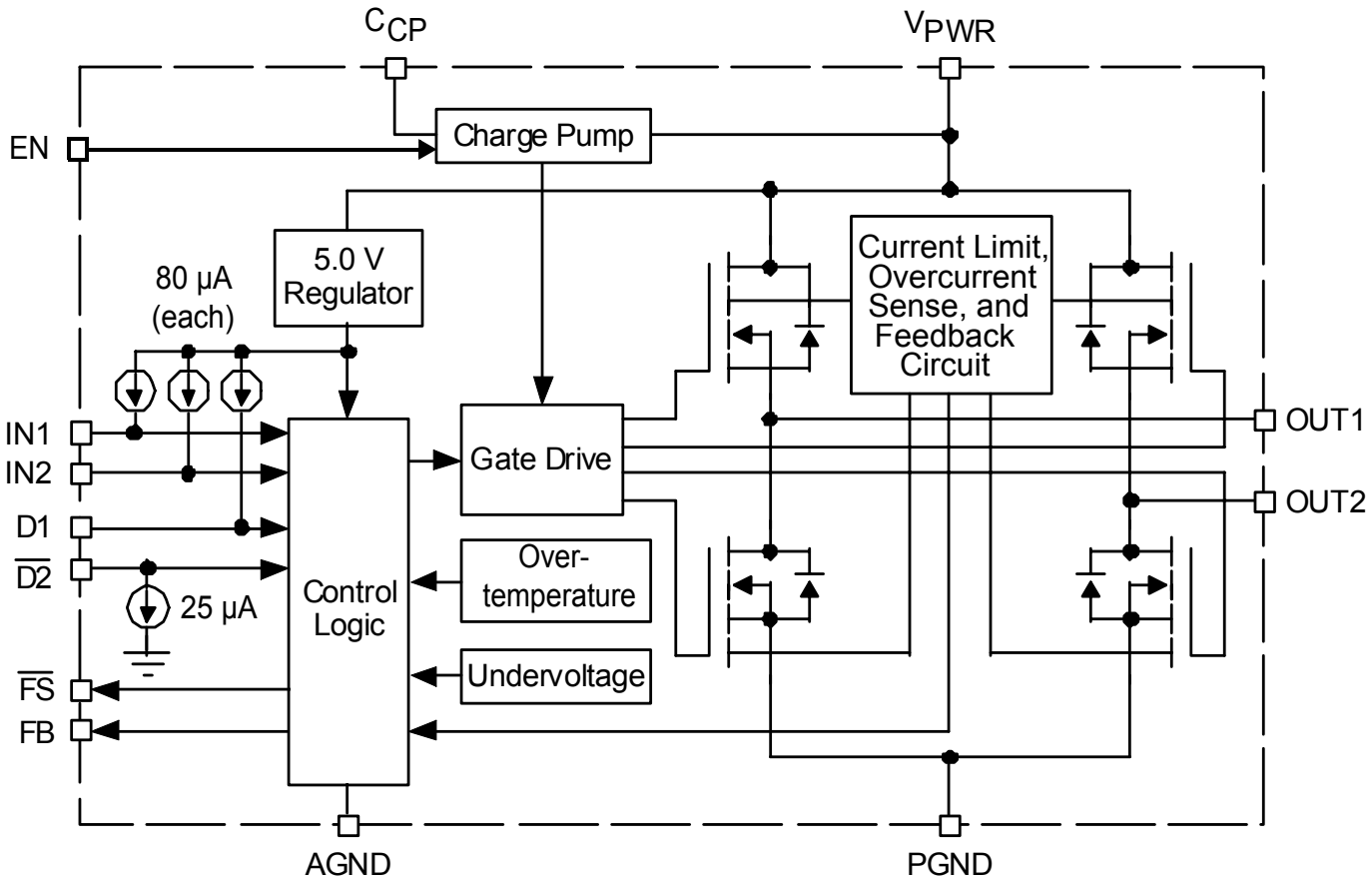
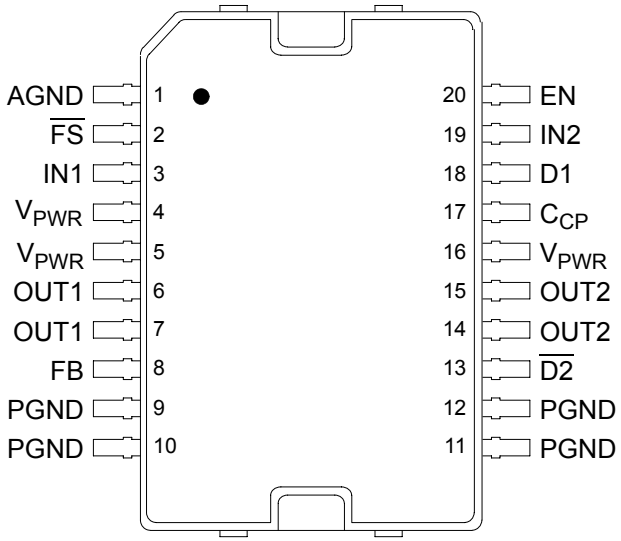
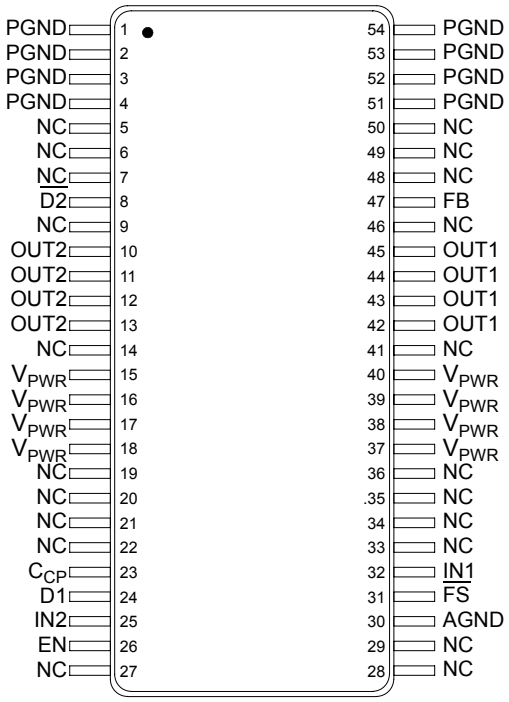


Figure 1. 33887 Internal Block Diagram



HSOP PIN FUNCTION DESCRIPTION

Pin	Pin Name	Description
1	AGND	Low current Analog signal ground.
2	$\overline{FS}$	Open drain active LOW Fault Status output requiring a pull-up resistor to 5.0 V.
3	IN1	Logic input control of OUT1 (i.e., IN1 logic HIGH = OUT1 HIGH).
4–5, 16	V_{PWR}	Positive power source connection.
6–7	OUT1	H-Bridge output 1.
8	FB	Current sensing feedback output providing ground referenced 1/375th (0.00266) of H-Bridge high-side output current.
9–12	PGND	Device high current power ground.
13	$\overline{D2}$	Active LOW input used to simultaneously tristate disable both H-Bridge outputs. When $\overline{D2}$ is Logic LOW, both outputs are tristate.
14–15	OUT2	H-Bridge output 2.
17	C_{CP}	External reservoir capacitor connection for internal Charge Pump.
18	D1	Active HIGH input used to simultaneously tristate disable both H-Bridge outputs. When D1 is Logic HIGH, both outputs are tristate.
19	IN2	Logic input control of OUT2 (i.e., IN2 logic HIGH = OUT2 HIGH).
20	EN	Logic input Enable control of device (i.e., EN logic High = Full Operation, EN logic LOW = Sleep Mode).



SOICW-EP PIN FUNCTION DESCRIPTION

Pin	Pin Name	Description
1–4, 51–54	PGND	Device high current power ground.
5–7, 9, 14, 19–22, 27–29, 33–36, 41, 46, 48–50	NC	No internal connection to this pin.
8	$\overline{D2}$	Active LOW input used to simultaneously tristate disable both H-Bridge outputs. When $\overline{D2}$ is Logic LOW, both outputs are tristate.
10–13	OUT2	H-Bridge output 2.
15–18, 37–40	V_{PWR}	Positive power source connection.
23	C_{CP}	External reservoir capacitor connection for internal Charge Pump.
24	D1	Active HIGH input used to simultaneously tristate disable both H-Bridge outputs. When D1 is Logic HIGH, both outputs are tristate.
25	IN2	Logic input control of OUT2 (i.e., IN2 logic HIGH = OUT2 HIGH).
26	EN	Logic input Enable control of device (i.e., EN logic HIGH = Full Operation, EN logic LOW = Sleep Mode).
30	AGND	Low current Analog signal ground.
31	$\overline{FS}$	Open drain active LOW Fault Status output requiring a pull-up resistor to 5.0 V.
32	IN1	Logic input control of OUT1 (i.e., IN1 logic HIGH = OUT1 HIGH).
42–45	OUT1	H-Bridge output 1.
47	FB	Current feedback output providing ground referenced 1/375th ratio of H-Bridge high-side output current.

MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
Power Supply Voltage			V
Normal Operation (Steady-State)	$V_{PWR(SS)}$	28	
Transient (Note 1)	$V_{PWR(t)}$	30 to 40	
Input Voltage (Note 2)	V_{IN}	7.0	V
$\overline{FS}$ Status Output (Note 3)	$V_{\overline{FS}}$	7.0	V
Continuous Output Current (Note 4)	$I_{OUT(CONT)}$	6.0	A
HSOP ESD Voltage			V
Human Body Model (Note 5)			
Each Pin to AGND	V_{ESD1}	±1000	
Each Pin to PGND	V_{ESD1}	±1500	
Each Pin to V_{PWR}	V_{ESD1}	±2000	
Each I/O to All Other I/Os	V_{ESD1}	±2000	
Machine Model (Note 6)	V_{ESD2}	±200	
SOICW-EP ESD Voltage			V
Human Body Model (Note 5)	V_{ESD1}	±1600	
Machine Model (Note 6)	V_{ESD2}	±200	
Storage Temperature	T_{STG}	-65 to 150	°C
Ambient Temperature (Note 7)	T_A	-40 to 125	°C
Operating Junction Temperature	T_J	-40 to 150	°C
Lead Soldering Temperature (Note 8)	T_{SOLDER}		°C
HSOP		220	
SOICW-EP		240	
Approximate Junction-to-Board Thermal Resistance (and package dissipation) (Note 7), (Note 9)	$R_{\theta J-B}$		°C/W
HSOP (6.0 W)		~5.0	
SOICW-EP (2.0 W)		~8.0	

Notes

1. Device will survive the transient overvoltage indicated for a maximum duration of 500 ms.
2. Exceeding the input voltage on IN1, IN2, EN, D1, or $\overline{D2}$ may cause a malfunction or permanent damage to the device.
3. Exceeding the pull-up resistor voltage on the open Drain $\overline{FS}$ pin may cause permanent damage to the device.
4. Continuous output current capability so long as junction temperature is ≤ 150°C.
5. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).
6. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
7. The limiting factor is junction temperature, taking into account the power dissipation, thermal resistance, and heat sinking.
8. Lead soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
9. Exposed heat sink pad plus the power and ground terminals comprise the main heat conduction paths. The actual $R_{\theta J-B}$ (junction-to-PC board) values will vary depending on solder thickness and composition and copper trace.

STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions 5.0 V ≤ V_{PWR} ≤ 28 V and -40°C ≤ T_A ≤ 125°C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Voltage Range (Note 10)					V
Steady-State	$V_{PWR(SS)}$	5.0	–	28	
Transient (t < 500 ms) (Note 11)	$V_{PWR(t)}$	–	–	40	
Sleep State Supply Current (Note 12)	$I_{PWR(sleep)}$				µA
V_{EN} = 0 V, I_{OUT} = 0 A		–	25	50	
Standby Supply Current	$I_{PWR(standby)}$				mA
I_{OUT} = 0 A, V_{EN} = 5.0 V		–	–	20	
Threshold Supply Voltage					
Switch-OFF	$V_{PWR(thres-OFF)}$	4.15	4.4	4.65	V
Switch-ON	$V_{PWR(thres-ON)}$	4.5	4.75	5.0	V
Hysteresis	$V_{PWR(hys)}$	150	–	–	mV
CHARGE PUMP					
Charge Pump Voltage	V_{CP} - V_{PWR}				V
V_{PWR} = 4.15 V		3.35	–	–	
V_{PWR} < 40 V		–	–	20	
CONTROL INPUTS					
Input Voltage (IN1, IN2, D1, $\overline{D2}$)					V
Threshold HIGH	V_{IH}	3.5	–	–	
Threshold LOW	V_{IL}	–	–	1.4	
Hysteresis	V_{HYS}	0.7	1.0	–	
Input Current (IN1, IN2, D1)	I_{IN}				µA
V_{IN} - 0.0 V		-200	-80	–	
Input Current ($\overline{D2}$, EN)	$I_{\overline{D2}}$				µA
$V_{\overline{D2}}$ = 5.0 V		–	25	100	

Notes

10. Development specifications are characterized over the range of 5.0 V ≤ V_{PWR} ≤ 28 V. Operation above 28 V may degrade device reliability.
11. Device will survive the transient overvoltage indicated for a maximum duration of 500 ms.
12. $I_{PWR(sleep)}$ is with sleep mode function Enabled.

STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions 5.0 V ≤ V_{PWR} ≤ 28 V and -40°C ≤ T_A ≤ 125°C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUTS (OUT1, OUT2)					
Output-ON Resistance (Note 13)	R_{OUT}				mΩ
5.0 V ≤ V_{PWR} ≤ 28 V, T_J = 25°C		–	120	–	
8.0 V ≤ V_{PWR} ≤ 28 V, T_J = 150°C		–	–	225	
5.0 V ≤ V_{PWR} ≤ 8.0 V, T_J = 150°C		–	–	300	
Output Latch-OFF Current	$I_{LATCH-OFF}$	5.2	6.5	7.8	A
High-Side Overcurrent Detection	$I_{OCD(H)}$	11	–	–	A
Low-Side Overcurrent Detection	$I_{OCD(L)}$	8.0	–	–	A
Leakage Current (Note 14)	$I_{OUT(leak)}$				μA
V_{OUT} = V_{PWR}		–	100	200	
V_{OUT} = GND		–	30	60	
Free-Wheeling Diode Forward Voltage Drop	V_F				V
I_{OUT} = 3.0 A		–	–	2.0	
Switch-OFF					°C
Thermal Shutdown	T_{LIM}	175	–	–	
Hysteresis	T_{HYS}	10	–	30	

Notes

13. Output-ON resistance as measured from output to V_{PWR} and GND.
14. Outputs switched OFF with D1 or $\overline{D2}$.

STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions 5.0 V ≤ V_{PWR} ≤ 28 V and -40°C ≤ T_A ≤ 125°C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
HIGH-SIDE CURRENT SENSE FEEDBACK					
Feedback Current	I_{FB}				
I_{OUT} = 0 mA		–	–	600	µA
I_{OUT} = 500 mA		1.07	1.33	1.60	mA
I_{OUT} = 1.5 A		3.6	4.0	4.4	mA
I_{OUT} = 3.0 A		7.2	8.0	8.8	mA
I_{OUT} = 6.0 A		14.4	16	17.6	mA
FAULT STATUS (Note 15)					
Fault Status Leakage Current (Note 16)	$I_{\overline{FS}(leak)}$				µA
$V_{\overline{FS}}$ = 5.0 V		–	–	10	
Fault Status SET Voltage (Note 17)	$V_{\overline{FS}(LOW)}$				V
$I_{\overline{FS}}$ = 300 µA		–	–	1.0	

Notes

15. Fault Status output is an open Drain output requiring a pull-up resistor to 5.0 V.
16. Fault Status Leakage Current is measured with Fault Status HIGH and *not* SET.
17. Fault Status Set Voltage is measured with Fault Status LOW and SET with $I_{\overline{FS}}$ = 300 µA.

DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions 5.0 V ≤ V_{PWR} ≤ 28 V and -40°C ≤ T_A ≤ 125°C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
TIMING CHARACTERISTICS					
PWM Frequency (Note 18)	f_{PWM}	–	10	–	kHz
Maximum Switching Frequency During Current Limit (Note 19)	f_{MAX}	–	–	20	kHz
Output ON Delay (Note 20) V_{PWR} = 14 V	$t_{d(ON)}$	–	–	18	µs
Output OFF Delay (Note 20) V_{PWR} = 14 V	$t_{d(OFF)}$	–	–	18	µs
Output Latch-OFF Time	t_a	15	20.5	26	µs
Output Blanking Time	t_b	12	16.5	21	µs
Output Rise and Fall Time (Note 21) V_{PWR} = 14 V, I_{OUT} = 3.0 A	t_f, t_r	2.0	5.0	8.0	µs
Overcurrent/Overtemperature Turn-OFF Time (Note 22)	t_{FAULT}	–	4.0	–	µs
Disable Delay Time (Note 23)	$t_{d(disable)}$	–	–	8.0	µs
Power-ON Delay Time (Note 24)	t_{pod}	–	1.0	5.0	ms
Wake-Up Delay Time (Note 24)	t_{wud}	–	1.0	5.0	ms
Free-Wheeling Diode Reverse Recovery Time (Note 25)	t_{rr}	100	–	–	ns

Notes

18. The outputs can be PWM controlled from an external source. This is typically done by holding one input high while applying a PWM pulse train to the other input. The maximum PWM frequency obtainable is a compromise between switching losses and switching frequency. Refer to Typical Switching Waveforms, Figures 8 through 15.
19. The Maximum Switching Frequency during Current Limit is internally implemented. The internal control produces a constant OFF-time PWM of the output. The output load characteristics affect the switching frequency.
20. Output Delay is the time duration from the midpoint of the IN1 or IN2 input signal to the 10% or 90% point (dependent on the transition direction) of the OUT1 or OUT2 signal. If the output is transitioning HIGH-to-LOW, the delay is from the midpoint of the input signal to the 90% point of the output response signal. If the output is transitioning LOW-to-HIGH, the delay is from the midpoint of the input signal to the 10% point of the output response signal. See Figure 3.
21. Rise Time is from the 10% to the 90% level and Fall Time is from the 90% to the 10% level of the output signal. See Figure 4.
22. Increasing output currents will become limited at 6.5 A. Hard shorts will breach the 6.5 A limit, forcing the output into an immediate tristate latch-OFF. See Figures 6 and 7. Output current limiting will cause junction temperatures to rise. A junction temperature above 160°C will cause the output current limit to progressively “fold-back”, or decrease, to 2.5 A typical at 175°C where thermal latch-OFF will occur. See Figure 5.
23. Disable Delay Time is the time duration from the midpoint of the D (disable) input signal to 10% of the output tristate response. See Figure 3.
24. Parameter has been characterized but not production tested.
25. Parameter is guaranteed by design but not production tested.

Timing Diagrams

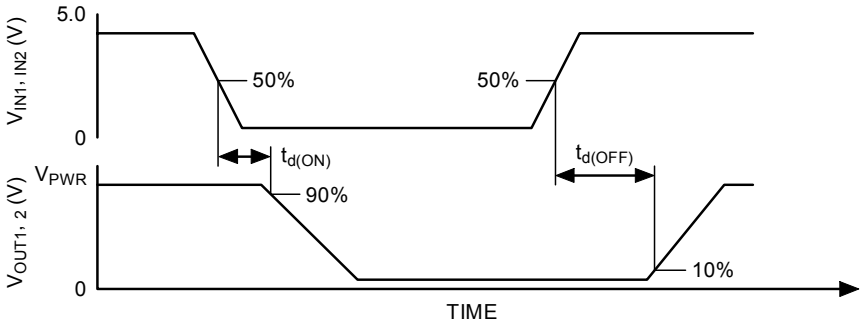


Figure 2. Output Delay Time

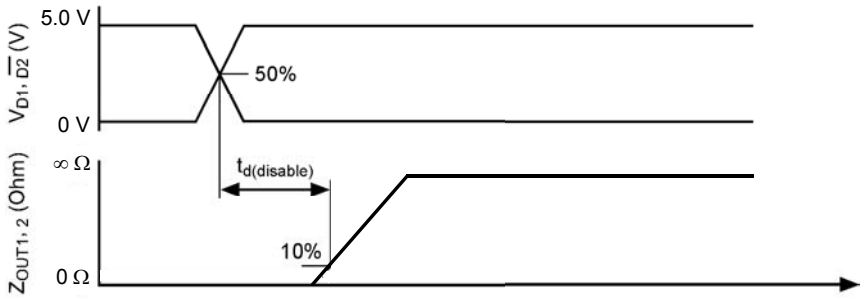


Figure 3. Disable Delay Time

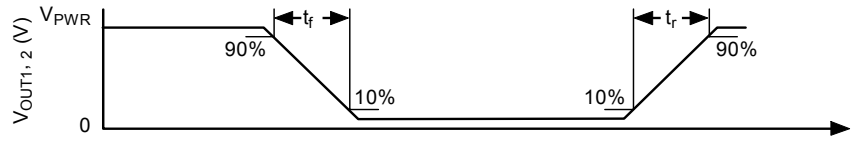


Figure 4. Output Switching Time

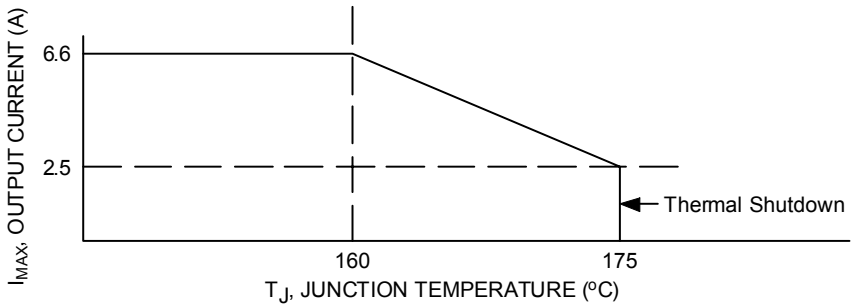


Figure 5. Output Current Limiting Versus Temperature (Typical)

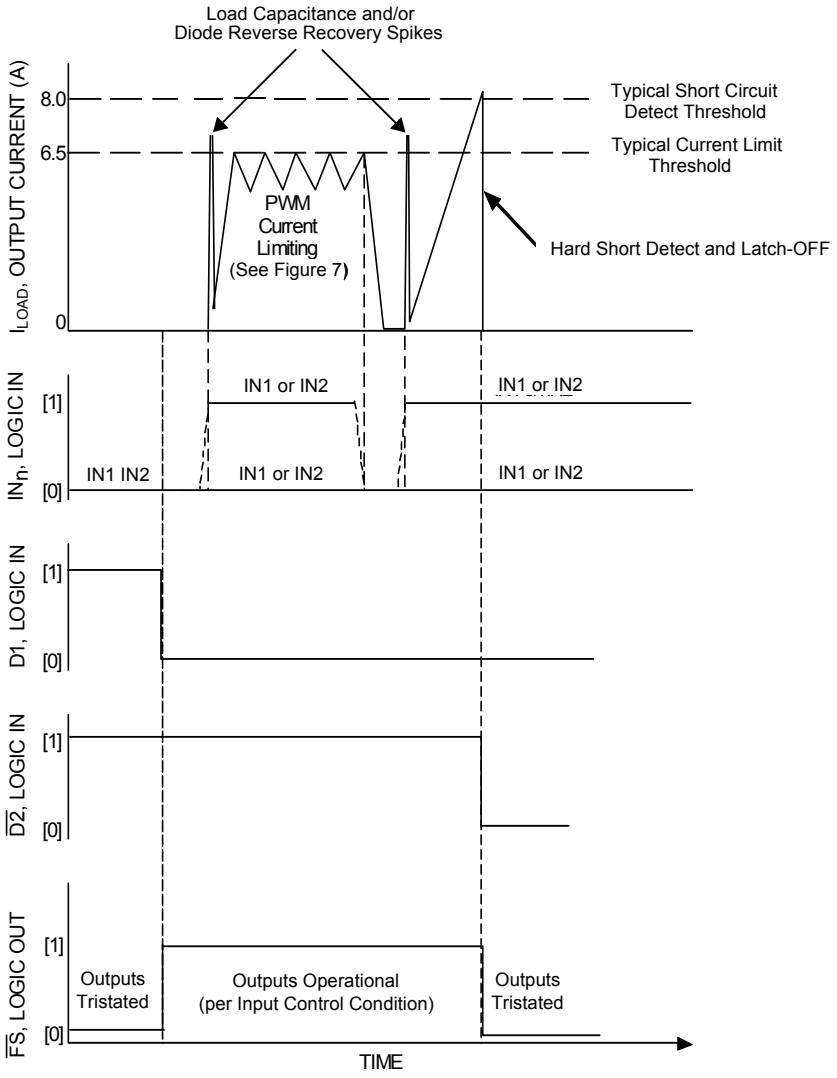


Figure 6. Output Load Current Limiting Versus Time

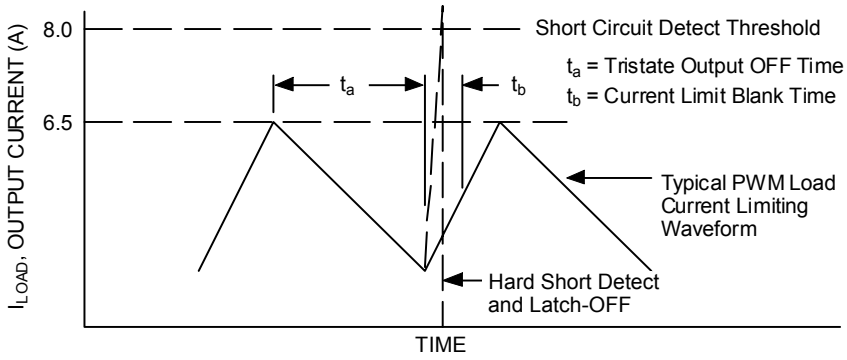


Figure 7. PWM Current Limiting Detail

Electrical Performance Curves
Typical Switching Waveforms

Important For all plots, the following applies:

- Ch2=2.0 A per division
- L_{LOAD}=533 µH @ 1.0 kHz
- L_{LOAD}=530 µH @ 10.0 kHz
- R_{LOAD}=4.0 Ω

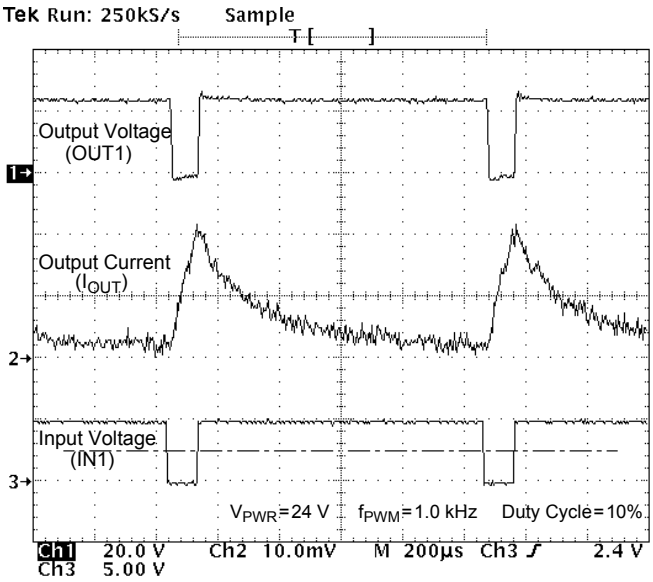


Figure 8. Output Voltage and Output Current vs. Input Voltage at V_{PWR}=24 V, PMW Frequency of 1.0 kHz, and Duty Cycle of 10%

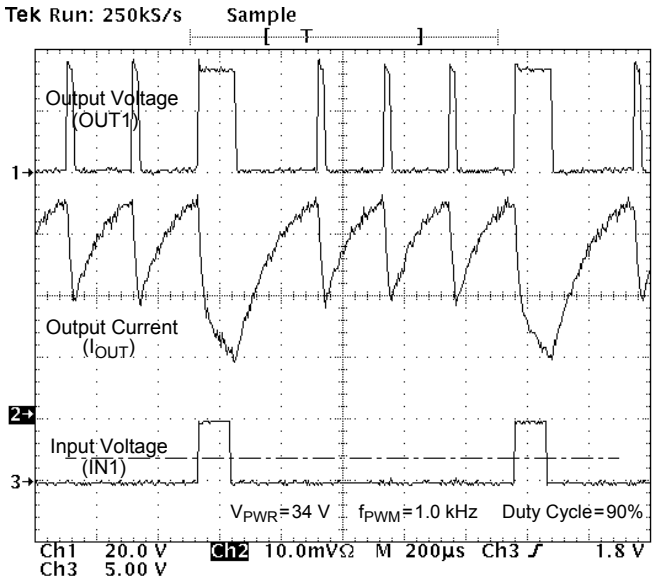


Figure 10. Output Voltage and Output Current vs. Input Voltage at V_{PWR}=34 V, PMW Frequency of 1.0 kHz, and Duty Cycle of 90%, Showing Device in Current Limiting Mode

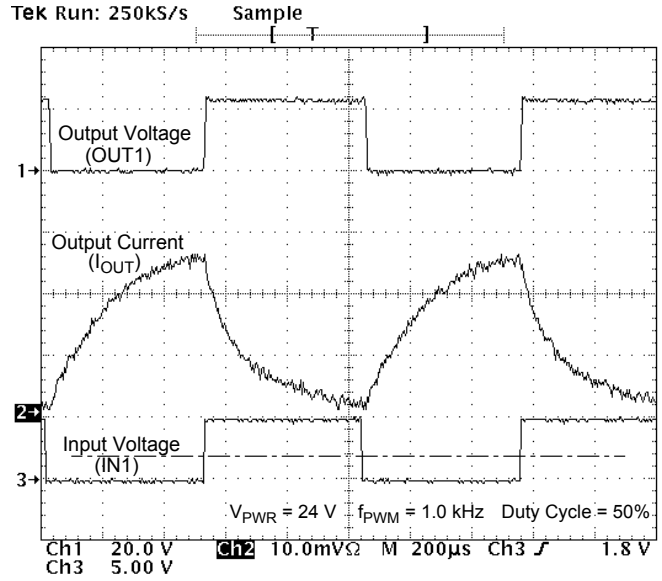


Figure 9. Output Voltage and Output Current vs. Input Voltage at V_{PWR}=24 V, PMW Frequency of 1.0 kHz, and Duty Cycle of 50%

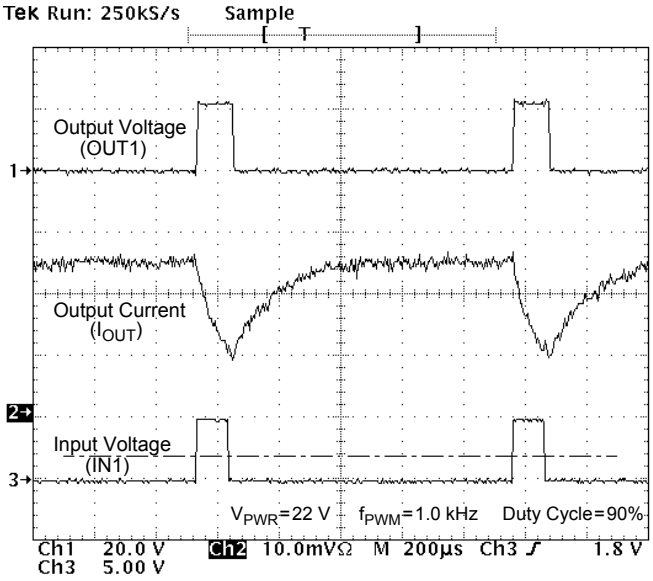


Figure 11. Output Voltage and Output Current vs. Input Voltage at V_{PWR}=22 V, PMW Frequency of 1.0 kHz, and Duty Cycle of 90%

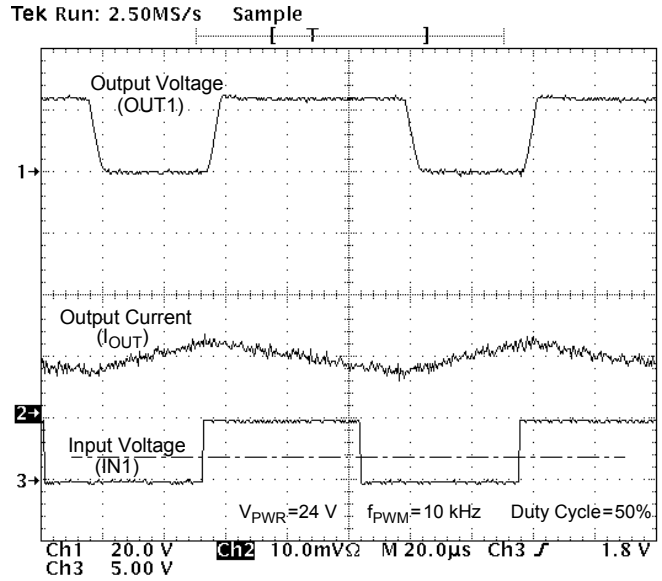


Figure 12. Output Voltage and Output Current vs. Input Voltage at V_{PWR}=24 V, PMW Frequency of 10 kHz, and Duty Cycle of 50%

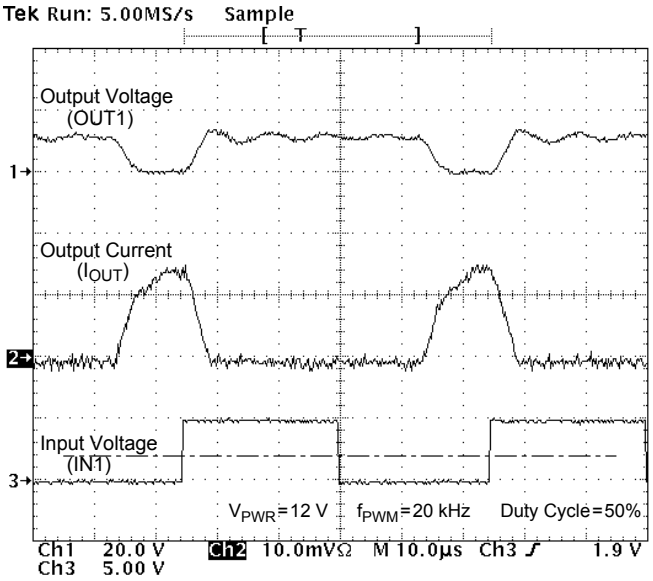


Figure 14. Output Voltage and Output Current vs. Input Voltage at V_{PWR}=12 V, PMW Frequency of 20 kHz, and Duty Cycle of 50% for a Purely Resistive Load

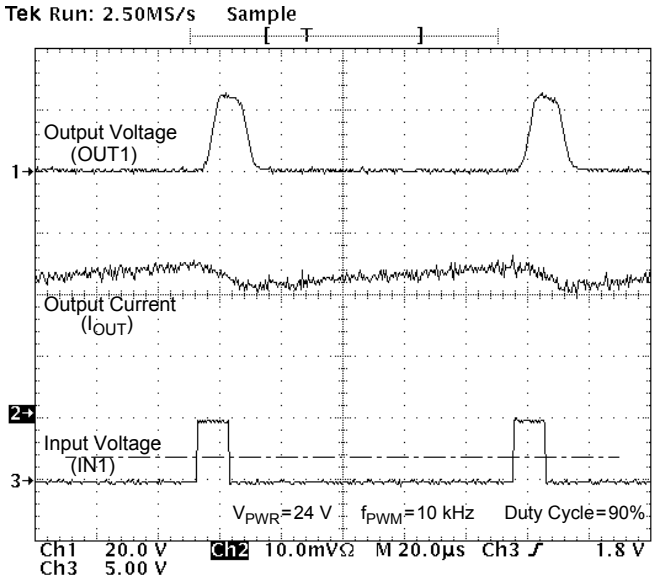


Figure 13. Output Voltage and Output Current vs. Input Voltage at V_{PWR}=24 V, PMW Frequency of 10 kHz, and Duty Cycle of 90%

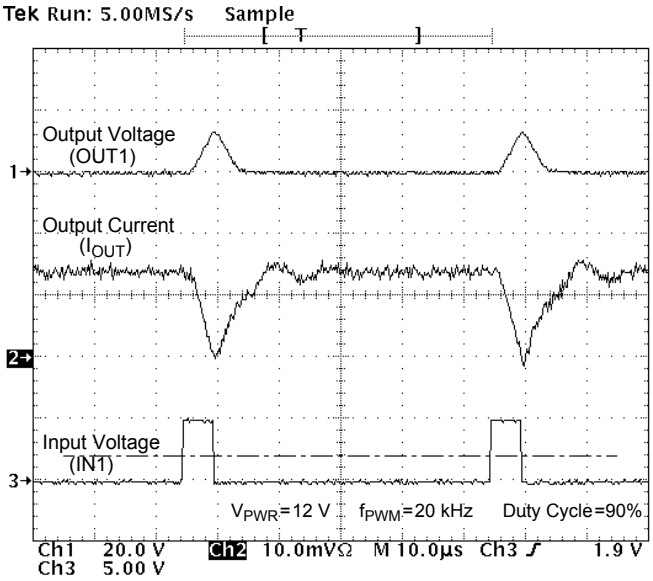


Figure 15. Output Voltage and Output Current vs. Input Voltage at V_{PWR}=12 V, PMW Frequency of 20 kHz, and Duty Cycle of 90% for a Purely Resistive Load

Table 1. Truth Table

The tristate conditions and the fault status are reset using D1 or $\overline{D2}$. The truth table uses the following notations: L = Low, H = High, X = High or Low, and Z = High impedance (all output power transistors are switched off).

Device State	EN	Input Conditions				Status	Outputs	
		D1	$\overline{D2}$	IN1	IN2	$\overline{FS}$	OUT1	OUT2
Forward	H	L	H	H	L	H	H	L
Reverse	H	L	H	L	H	H	L	H
Free Wheeling Low	H	L	H	L	L	H	L	L
Free Wheeling High	H	L	H	H	H	H	H	H
Disable 1 (D1)	H	H	X	X	X	L	Z	Z
Disable 2 ($\overline{D2}$)	H	X	L	X	X	L	Z	Z
IN1 Disconnected	H	L	H	Z	X	H	H	X
IN2 Disconnected	H	L	H	X	Z	H	X	H
D1 Disconnected	H	Z	X	X	X	L	Z	Z
$\overline{D2}$ Disconnected	H	X	Z	X	X	L	Z	Z
Undervoltage (Note 26)	H	X	X	X	X	L	Z	Z
Overtemperature (Note 27)	H	X	X	X	X	L	Z	Z
Overcurrent (Note 27)	H	X	X	X	X	L	Z	Z
Sleep Mode EN	L	X	X	X	X	H	Z	Z
EN Disconnected	Z	X	X	X	X	H	Z	Z

Notes

26. In the case of an undervoltage condition, the outputs tristate and the fault status is SET logic LOW. Upon undervoltage recovery, fault status is reset automatically or automatically cleared and the outputs are restored to their original operating condition.
27. When an overcurrent or overtemperature condition is detected, the power outputs are tristate latched-OFF independent of the input signals and the fault status flag is SET logic LOW.

SYSTEM/APPLICATION INFORMATION

INTRODUCTION

Numerous protection and operational features (speed, torque, direction, dynamic breaking, PWM control, and closed-loop control), in addition to the 5.2 A rms output current capability, make the 33887 a very attractive, cost-effective solution for controlling a broad range of small DC motors. In addition, a pair of 33887 devices can be used to control bipolar stepper motors. The 33887 can also be used to excite transformer primary windings with a switched square wave to produce secondary winding AC currents.

As shown in Figure 1, Internal Block Diagram, the 33887 is a fully protected monolithic H-Bridge with Enable, Fault Status reporting, and High-Side current sense feedback to accommodate closed-loop PWM control. For a DC motor to run, the input conditions need be as follows: Enable input logic HIGH, D1 input logic LOW, $\overline{D2}$ input logic HIGH, $\overline{FS}$ flag cleared (logic HIGH), one IN logic LOW and the other IN logic HIGH (to define output polarity). The 33887 can execute Dynamic Breaking by simultaneously turning on either both High-Side MOSFETs or both Low-Side MOSFETs in the output H-Bridge; e.g., IN1 and IN2 logic HIGH or IN1 and IN2 logic LOW.

The 33887 outputs are capable of providing a continuous DC load current of 5.2 A from a 28 V V_{PWR} source. An internal charge pump supports PWM frequencies to 10 kHz. An external pull-up resistor is required at the $\overline{FS}$ pin for fault status reporting. The 33887 has an analog feedback (current mirror) output pin (the FB pin) that provides a constant-current source ratioed to the active high-side MOSFET. This can be used to provide “real time” monitoring of output current to facilitate closed-loop operation for motor speed/torque control.

Two independent inputs (IN1 and IN2) provide control of the two totem-pole half-bridge outputs. Two disable inputs (D1 and $\overline{D2}$) provide the means to force the H-Bridge outputs to a high impedance state (all H-Bridge switches OFF). An EN pin controls an enable function that allows the 33887 to be placed in a power-conserving sleep mode.

The 33887 has Undervoltage Shutdown with automatic recovery, Output Current Limiting, Output Short-Circuit Latch-OFF, and Overtemperature Latch-OFF. An Undervoltage Shutdown, Output Short-Circuit Latch-OFF, or Overtemperature Latch-OFF fault condition will cause the outputs to turn OFF (i.e., become high impedance or tristated) and the fault output flag to be set LOW. Either of the Disable inputs or V_{PWR} must be “toggled” to clear the fault flag.

Current limiting is accomplished by a constant-off-time PWM method employing current limit threshold triggering. The current limiting scheme is unique in that it incorporates a junction-temperature dependent current-limit threshold. This means the current limit threshold is “ramped down” as the junction temperature increases above 160°C, until at 175°C the output current will have been decreased to about 2.5 A. Above 175°C, the Overtemperature Shutdown (Latch-OFF) occurs. This combination of features allows the device to remain in operation for a longer period of time with unexpected loads, while still retaining adequate protection for both the device and the load.

FUNCTIONAL PIN DESCRIPTION

PGND and AGND

Power and analog ground pins. The power and analog ground pins should be connected together with a very low impedance connection.

V_{PWR}

V_{PWR} pins are the power supply inputs to the device. All V_{PWR} pins must be connected together on the printed circuit board with as short as possible traces offering as low impedance as possible between pins.

V_{PWR} pins have an undervoltage threshold. If the supply voltage drops below a V_{PWR} undervoltage threshold, the output power stage switches to a tristate condition and the fault status flag is SET and the Fault Status pin voltage switched to a logic LOW. When the supply voltage returns to a level that is above the threshold, the power stage automatically resumes normal operation according to the established condition of the input pins and the fault status flag is automatically reset logic HIGH.

Fault Status ($\overline{FS}$)

This pin is the device fault status output. This output is an active LOW open drain structure requiring a pull-up resistor to 5.0 V. Refer to Table 1, Truth Table, page 14.

IN1, IN2, D1, and $\overline{D2}$

These pins are input control pins used to control the outputs. These pins are 5.0 V CMOS-compatible inputs with hysteresis. The IN1 and IN2 independently control OUT1 and OUT2, respectively. D1 and $\overline{D2}$ are complementary inputs used to tristate disable the H-Bridge outputs.

When either D1 or $\overline{D2}$ is SET (D1 = logic HIGH or $\overline{D2}$ = logic LOW) in the disable state, outputs OUT1 and OUT2 are both tristate disabled; however, the rest of the device circuitry is fully operational and the supply $I_{PWR(standby)}$ current is reduced to a few milli-amperes. Refer to Table 1, Truth Table, and STATIC ELECTRICAL CHARACTERISTICS table.

OUT1 and OUT2

These pins are the outputs of the H-Bridge with integrated free-wheeling diodes. The bridge output is controlled using the IN1, IN2, D1, and $\overline{D2}$ inputs. The outputs have pulse width modulated (PWM) current limiting above 6.5 A. The outputs also have thermal shutdown (tristate latch-OFF) with hysteresis as well as short circuit latch-OFF protection.

A disable timer (time t_b) incorporated to detect currents that are higher than current limit is activated at each output activation to facilitate hard short detection (see Figure 7).

C_{CP}

Charge pump output pin. A filter capacitor (up to 33 nF) can be connected from the C_{CP} pin and PGND. The device can operate without the external capacitor, although the C_{CP} capacitor helps to reduce noise and allows the device to perform at maximum speed, timing, and PWM frequency.

EN

The EN pin is used to place the device in a sleep mode so as to consume very low currents. When the EN pin voltage is a logic LOW state, the device is in the sleep mode. The device is enabled and fully operational when the EN pin voltage is logic HIGH. An internal pull-down resistor maintains the device in sleep mode in the event EN is driven through a high impedance I/O or an unpowered microcontroller, or the EN input becomes disconnected.

FB

The device has a feedback output (FB) for “real time” monitoring of H-Bridge high-side output currents to facilitate closed-loop operation for motor speed and torque control.

The FB pin provides current sensing feedback of the H-Bridge high-side drivers. When running in the forward or reverse direction, a ground referenced 1/375th (0.00266) of load current is output to this pin. Through the use of an external resistor to ground, the proportional feedback current can be converted to a proportional voltage equivalent and the controlling microcontroller can “read” the current proportional voltage with its analog-to-digital converter (ADC). This is intended to provide the user with motor current feedback for motor torque control. The accuracy is ±20% at load currents <1.5 A and ±10% at load currents >1.5 A.

If PWM-ing is implemented using the disable pin inputs (either D1 or $\overline{D2}$), a small filter capacitor (<1.0 µF) may be required in parallel with the external resistor to ground for fast spike suppression.

PERFORMANCE FEATURES

Short Circuit or Overcurrent Protection

If an output overcurrent condition is detected, the power outputs tristate (latch-OFF) independent of the input (IN1 and IN2) states, and the fault status output flag is SET logic LOW. If the D1 input changes from logic HIGH to logic LOW, or if the $\overline{D2}$ input changes from logic LOW to logic HIGH, the output bridge will become operational again and the fault status flag will be reset (cleared) to a logic HIGH state.

The output stage will always switch into the mode defined by the input pins (IN1, IN2, D1, and $\overline{D2}$), provided the device junction temperature is within the specified operating temperature range.

PWM Current Limiting

The maximum current flow under normal operating conditions is limited to I_{MAX} (5.2 A to 7.8 A). When the maximum current value is reached, the output stages are tristated for a fixed time (t_a) of 20 µs typical. Depending on the time constant associated with the load characteristics, the output current decreases during the tristate duration until the next output ON cycle occurs (see Figures 7 and 10).

The PWM current limit threshold value is dependent upon the device junction temperature. When $-40°C \le T_J \le 160°C$, I_{MAX} is between 5.2 A to 7.8 A. When T_J exceeds 160°C, the I_{MAX} current decreases linearly down to 2.5 A typical at 175°C. Above 175°C the device overtemperature circuit detects T_{LIM} and overtemperature shutdown occurs (see Figure 5). This feature allows the device to remain operational for a longer time but at a regressing output performance level at junction temperatures above 160°C.

Overtemperature Shutdown and Hysteresis

If an overtemperature condition occurs, the power outputs are tristated (latched-OFF) and the fault status flag is SET to logic LOW.

To reset from this condition, D1 must change from logic HIGH to logic LOW, or $\overline{D2}$ must change from logic LOW to logic HIGH. When reset, the output stage switches ON again, provided that the junction temperature is now below the overtemperature threshold limit minus the hysteresis.

Note Resetting from the fault condition will clear the fault status flag.

APPLICATIONS

A typical application schematic is shown in Figure 16. For precision high-current applications in harsh, noisy environments, the V_{PWR} by-pass capacitor may need to be substantially larger.

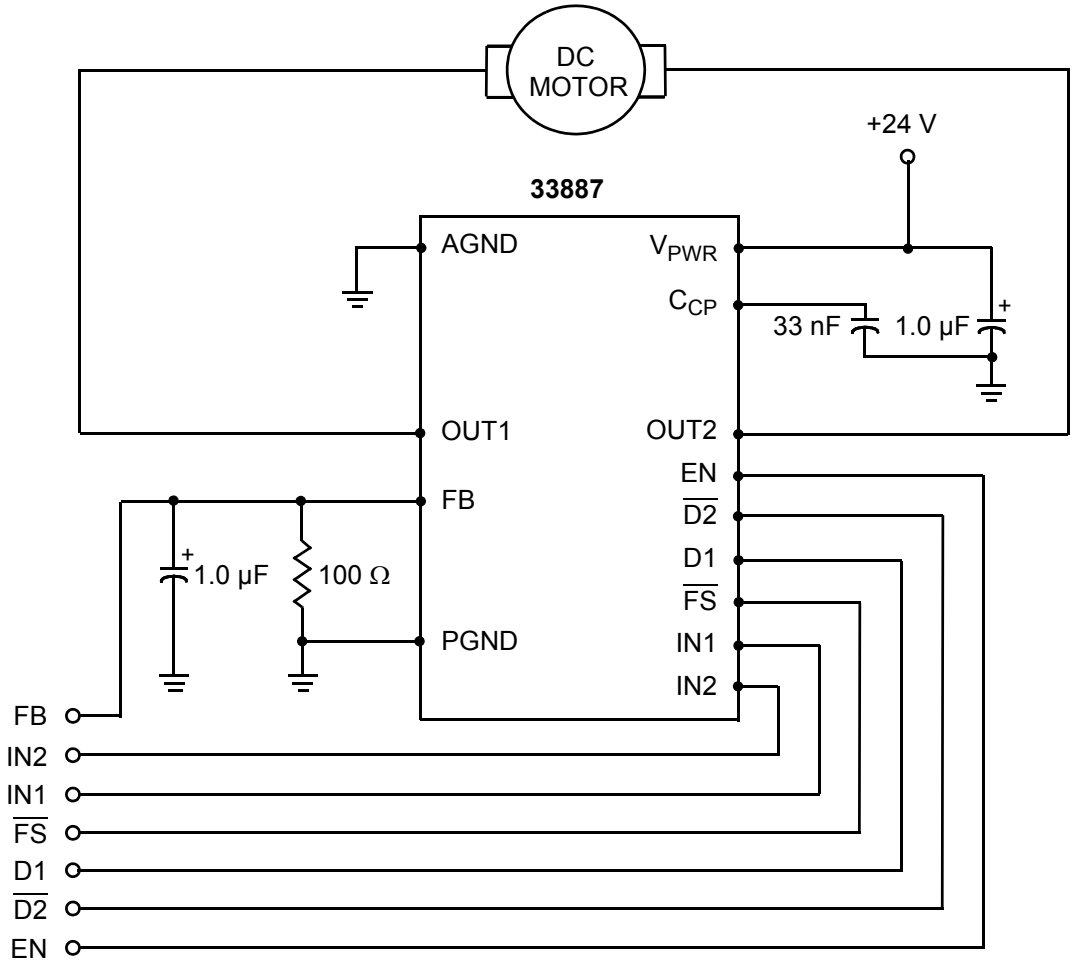
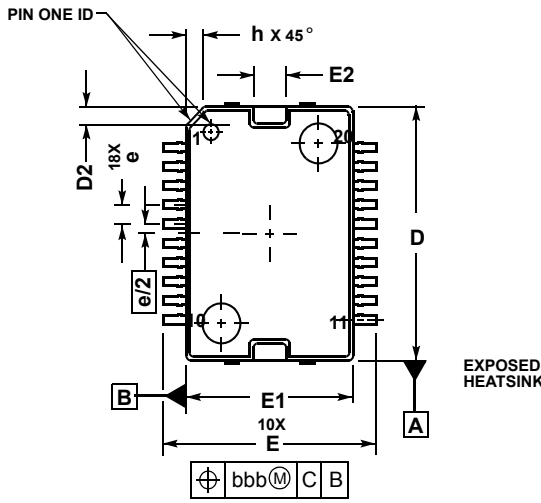


Figure 16. Typical Application Schematic

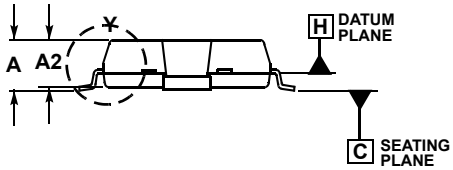
PACKAGE DIMENSIONS

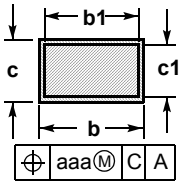
DH SUFFIX
(20-LEAD HSOP)
PLASTIC PACKAGE
CASE 979C-02
ISSUE A



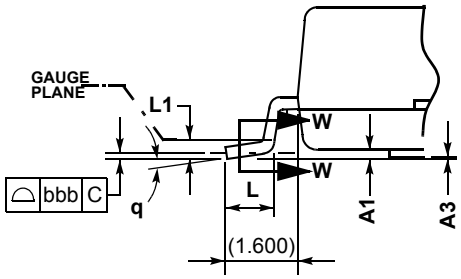
BOTTOM VIEW

NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.150 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE TIEBAR PROTRUSIONS. ALLOWABLE TIEBAR PROTRUSIONS ARE 0.150 PER SIDE.





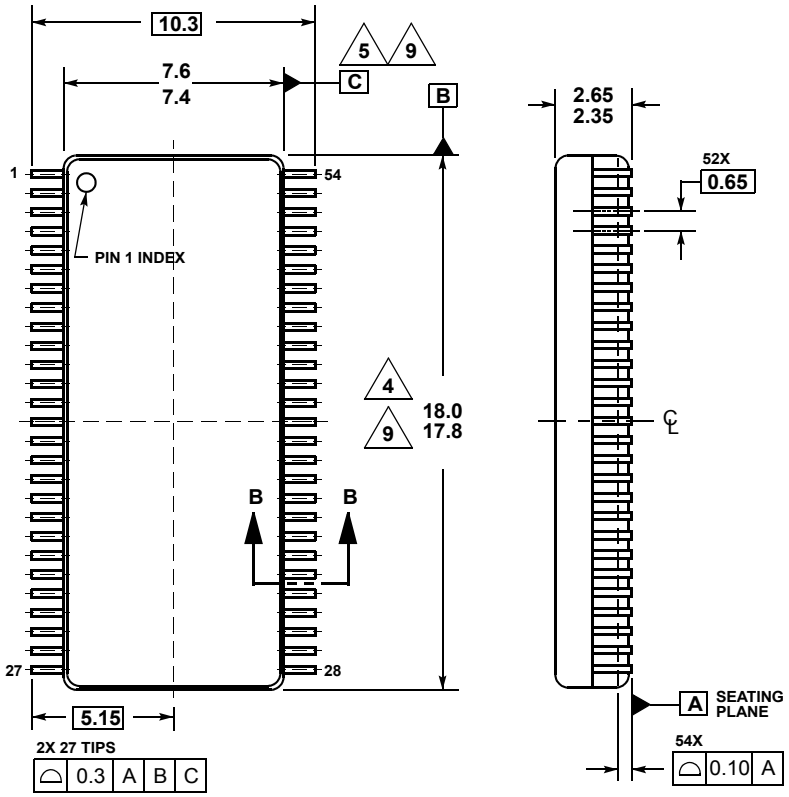
SECTION W-W



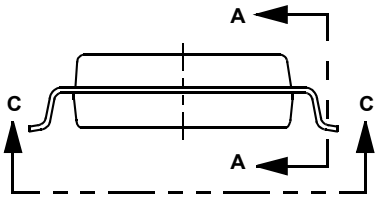
DETAIL Y

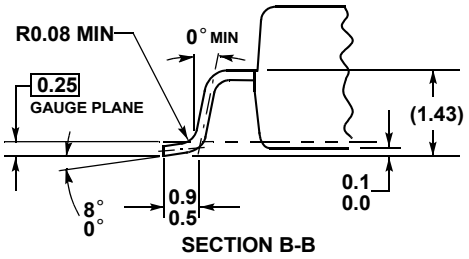
DIM	MILLIMETERS MIN	MAX
A	3.000	3.400
A1	0.100	0.300
A2	2.900	3.100
A3	0.00	0.100
D	15.800	16.000
D1	11.700	12.600
D2	0.900	1.100
E	13.950	14.450
E1	10.900	11.100
E2	2.500	2.700
E3	6.400	7.200
E4	2.700	2.900
L	0.840	1.100
L1	0.350 BSC	
b	0.400	0.520
b1	0.400	0.482
c	0.230	0.320
c1	0.230	0.280
e	1.270 BSC	
h	---	1.100
q	0 °	8 °
aaa	0.200	
bbb	0.100	

DWB SUFFIX
(54-LEAD SOICW EXPOSED PAD)
PLASTIC PACKAGE
CASE 1390-01
ISSUE B

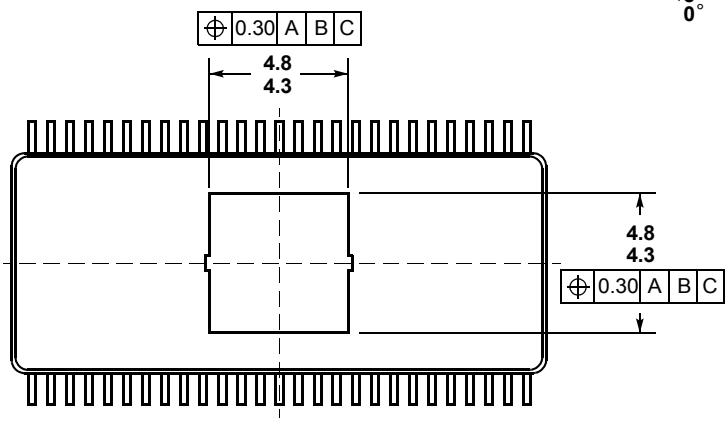


NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 MM.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.3 MM FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER-LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

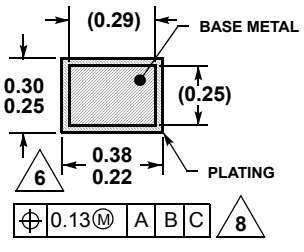




SECTION B-B



VIEW C-C



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